Ankit Gupta, R. S. Gamad/ International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 1, Issue 2, pp.122-124

Design Of A Single Stage Source Coupled CMOS VCO using 180nm Technology

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ABSTRACT

A single stage source coupled Complementary Metal Oxide Semiconductor Voltage Controlled Oscillator (CMOS VCO) is designed in this paper. The design is implemented in Cadence environment with high oscillation frequency and low power consumption. This design is a single stage and it has low phase noise because author has reduced noise sources. Oscillation frequency of the designed VCO is ranges from 1.052 GHz to 2.136 GHz. The circuit is simulated using 180nm UMC Technology. Simulation results are reported that the phase noise is -64.96dBc/Hz@1MHz and power consumption is 6.951 mW with 2.136 GHz oscillation frequency and 1.8 V supply voltage. Present results are compared with earlier published work and improvements are observed.

Keywords - Cadence, Low power, Low Phase Noise, Source coupled VCO

I. INTRODUCTION

VCO is the heart of the Phase Locked Loops (PLLs) and data recovery circuits which is widely used in wireless and wire-line communication system. In recent years, the CMOS LC-tank oscillators have shown an excellent phase noise performance with Low power consumption because of a relatively high quality factor [1]. The oscillation frequency of the ring oscillator is inversely proportional to the number of delay stages. It is desirable to design a two stage ring VCO to satisfy Barkhausens criteria. Several novel delay cells have been proposed to compose the two stage ring VCO [2][3]. But much extra power is needed to provide an excess phase shift. The output signal swing is reduced in order to place the complex poles in front of the zero. Consequently, the phase noise performance of this two stage ring VCO is relatively poor [4].

II. INDENTATIONS AND EQUATIONS

The Frequency of Oscillation is given as [7]:

Initially we have mathematical analysis

$$F_{osc} = 1/2.\ \Delta t = I_d / 4.C.\ V_{th} \qquad (1)$$

where F_{osc}= the frequency of oscillation.

The average power dissipated by the VCO is

$$P_{avg} = VDD.\ I_{avg} = VDD.\ I_D \qquad (2)$$

Where, VDD = supply voltage and I_D = drain current through supply voltage

III. FIGURES AND TABLES

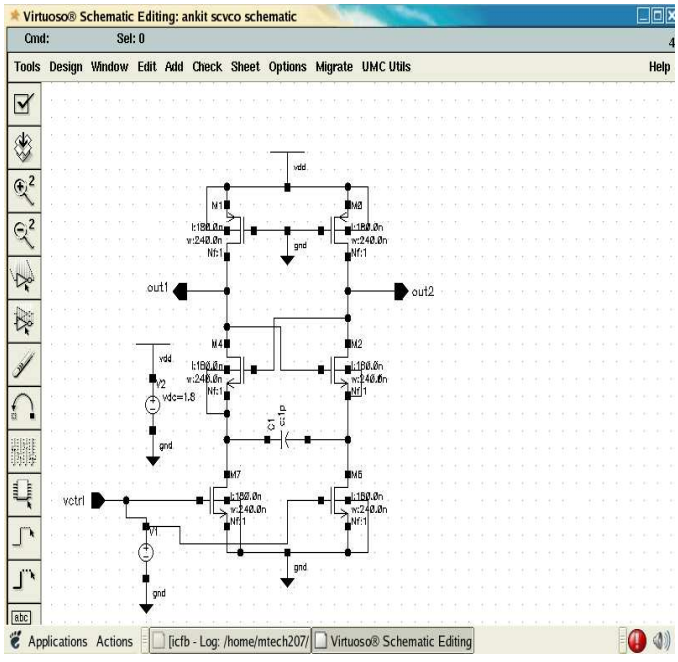

Fig.1 schematic design view of the VCO

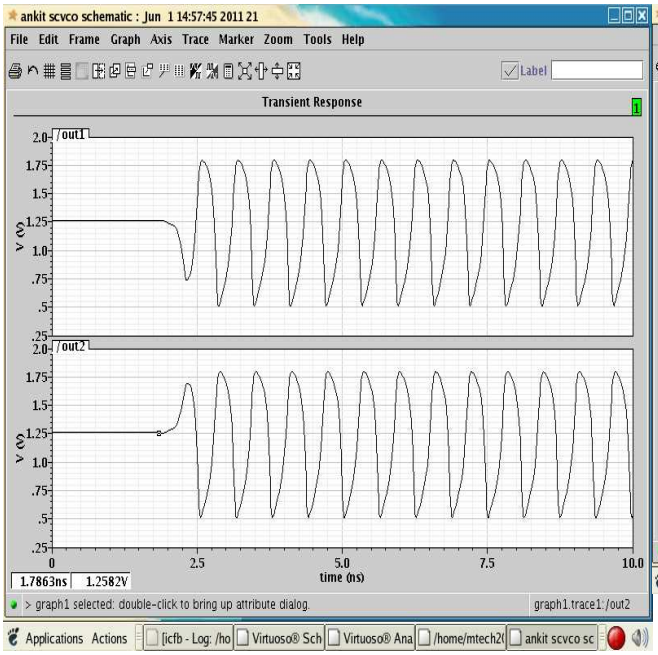

Fig.2 Simulation result of the output VCO

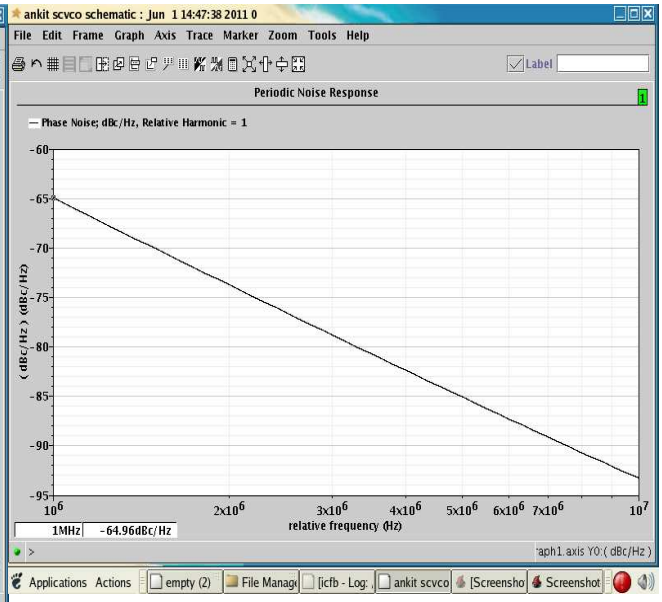

Fig.4 Results of the Phase Noise

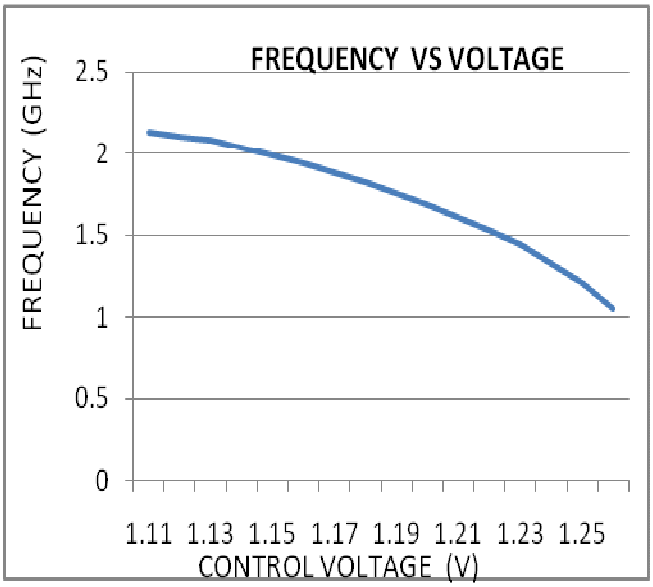

Fig.3 Graphical representation of frequency Vs control Voltage

Table 1: Comparison of present work with earlier reported work

parameter	Ref[1]	Ref[5]	This design
Operating Voltage	1.8V	3.3V	1.8V
Techno. (CMOS)	0.18µm (CMOS Techno.)	0.35µm (CMOS Techno.)	0.18µm (CMOS Techno.)
Power Consump.	17mW	15.5mW	6.951mW
Operating Frequency	2.5-5.2 GHz	2.5-5.2 GHz	1.052-2.136 GHz
Phase Noise (dBc/Hz)	-90.1dBc/Hz @1MHz	-135dBc/Hz @ 1MHz	-64.96dBc /Hz @1MHz
Number of stages	2	--	1

IV. CONCLUSION

This paper presents a design of a low power, low phase noise 2.136 GHz CMOS VCO using 180 nm UMC Technology. Finally authors have compared the presented results with earlier published work

and improvement observed in this result as given in table1. The simulation results of this design shows that the proposed VCO could achieve high oscillation frequency with the better phase noise performance and low power consumption. This design is suitable for wireless applications.

ACKNOWLEDGEMENTS

This work has been carried out in SMDP VLSI laboratory of the Electronics and Instrumentation Engineering Department of Shri G. S. Institute of Technology and Science, Indore, India. This SMDP VLSI project is funded by Ministry of Information and Communication Technology, Government of India. Authors are thankful to the Ministry for the facilities provided under this project.

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